module binary\_to\_gray\_test\_1;

// Inputs

reg [2:0] data\_in;

// Outputs

wire [2:0] data\_out;

// Instantiate the Unit Under Test (UUT)

binary\_to\_gray uut (

.data\_in(data\_in),

.data\_out(data\_out)

);

always # 10 data\_in[0] = ~data\_in[0];

always # 20 data\_in[1] = ~data\_in[1];

always # 40 data\_in[2] = ~data\_in[2];

initial begin

data\_in = 3'b000;

/\*data\_in = 4'b1100;#100;

data\_in = 4'b0111;#100;

data\_in = 4'b0011;#100;\*/

end

endmodule